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IN THE UNITED STATE PATENT AND TRADEMARK OFFICE

In re Patent application of	:	
Jae-Jun Lee et al.	:	Group Art Unit 2185
Serial No. 10/629,866	:	Examiner Daniel Y. Kim
Filed July 30, 2003	:	

Title: MEMORY SYSTEM HAVING MEMORY MODULES WITH DIFFERENT MEMORY DEVICE LOADS

SUBMISSION OF ENGISH LANGUAGE TRANSLATION OF FOREIGN-LANGUAGE PRIORITY APPLICATION

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Sir:

I, Nakjung Kim, declare and say:
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that the attached document represents an accurate English language translation of Korean Patent Application No. 2002-0045914, filed August 2, 2002.

Signed this 17 day of January, 2006.

(signature of translator)

[ABSTRACT]

[Abstract of the Disclosure]

The present invention discloses a memory system having a single in-line memory module (SIMM) and a dual in-line memory module (DIMM), each containing a plurality of memory devices, wherein a signal transmission line in the SIMM is longer than that in the DIMM to compensate signal delay time difference caused by an asymetrical structure that is formed due to the different numbers of loads in the SIMM and DIMM, thereby improving signal integrity of the memory system. Further, the memory system is able to compensate the signal delay time caused by a signal transmission line formed between a first socket where the SIMM type memory module is received and a second socket where the DIMM type memory module is recived, thereby improving the signal integrity.

[Representative Drawing]

Fig.1

[SPECIFICATION]

[Title of the Invention]

MEMORY SYSTEM WITH A SINGLE IN-LINE MEMORY MODULE (SIMM) AND A DUAL IN-LINE MEMORY MODULE (DIMM)

[Brief Description of the Drawings]

These and other features and advantages of the present invention will be readily apparent to those of ordinary skill in the art upon review of the detailed description that follows when taken in conjunction with the accompanying drawings, in which like reference numerals denote like parts, and in which:

FIG. 1 illustrates a block diagram of a memory system having a SIMM and a DIMM in accordance with the present invention,

FIG. 2 illustrates waveforms as a simulation result of the signal integrity of the memory system in FIG. 1, wherein the simulation is performed assuming the DIMM and the SIMM have the same length of the signal transmission line, and

FIG. 3 illustrates waveforms as a simulation result of signal integrity of the memory system shown in FIG. 1, wherein the simulation is performed assuming the DIMM and the SIMM have different lengths of signal transmission lines.

[Detailed Description of the invention]

[Object of the Invention]

[Technical field of the invention and Related Art prior to the Invention]

The present invention relates to a memory system, more particularly to the memory system having different types of memory modules such as a dual in-line memory module (DIMM) and a single in-line memory module (SIMM), and capable of improving signal integrity on a memory bus channel.

Generally, a computer memory system comprises a memory controller chip set, a plurality of memory devices, a plurality of resistors and wires those of which are mounted on a computer main board. The wires electrically connect the memory controller chip set, the memory devices and the resistors. The memory devices are mounted on the main board in a manner of module.

The memory module mounted on the main board acts as a load on the memory bus channel that is a data or signal transmission line between the memory controller chip set and the memory devices, thereby deteriorating electrical characteristic of the channels. That is, bandwidth of the memory bus channel is narrowed due to parasitic components of each device on the main board and impedance mismatching is caused. Further, signal integrity is deteriorated, so that distortion and modification of signals passing through the memory bus channels is occurred when the memory system is operated at high speed.

A plurality of memory bus channel structures has been suggested for preventing the signal integrity from being deteriorated in the memory system operating at high speed. Among those channel structures, there is a stub type channel used in wide for a memory DQ channel. In the stub type channel structure, a series resistor or a parallel capacitor is provided between the memory controller chip set and a first memory

module, and a channel stop resistor is provided at an end of the memory channel. The stub type channel structure reduces reflected wave that is generated due to the impedance mismatching, so that channel noises decrease greatly and the signal integrity is improved.

However, the stub type channel structure may not improve the signal integrity enough when the stub type channel structure is adapted in a memory system having both of the SIMM and DIMM. In the conventional memory system having the SIMM and DIMM therein, the SIMM and the DIMM has the different numbers of the loads, respectively, whereas the channel structure and a channel length are the same in the DIMM and the SIMM. Accordingly, signals are reached to each memory module with different delay times.

That is, when the stub type channel structure is adapted in the memory system, the signal integrity is degraded more severely in the memory system having different types of memory modules, for example the SIMM and the DIMM, than the memory system having one type of memory modules, the SIMM or the DIMM. The more the memory system operation speed is higher, the more the signal integrity is important.

[Technical Goal of the Invention]

In an effort to overcome the problems described above, it is a feature of an embodiment of the present invention to provide a memory system having a SIMM and a DIMM and capable of improving signal integrity on a memory bus channel by

configuring the memory modules in a way that an internal signal transmission line of the SIMM is longer than that of the DIMM.

[Structure and Operation of the Invention]

In accordance with one aspect of the present invention, there is provided a memory system having a SIMM and a DIMM, each containing a plurality of memory devices, wherein a signal transmission line in the SIMM type memory module is longer than a signal transmission line in the DIMM to compensate signal delay time difference caused by the different numbers of the memory devices contained in the SIMM and the DIMM, whereby improving signal integrity.

The memory system is able to compensate the signal delay time caused by signal transmission lines formed between a first socket for receiving the SIMM and a second socket for receiving the DIMM, whereby improving signal integrity.

Korean Patent Application No. 2002-45914, filed August 2, 2002 and entitled: "Memory System" is hereby incorporated by reference in its entirety.

Reference will now be made in detail to preferred embodiments of the present invention, an example of which is illustrated in the accompanying drawings.

FIG. 1 illustrates a block diagram of a memory system in accordance with the present invention. As shown in FIG. 1, the memory system includes a SIMM and a DIMM. There may be a plurality of semiconductor devices in the memory system but only semiconductor devices connected to a DQ channel are illustrated in FIG. 1.

The memory system of the present invention includes a memory controller 10, a

first socket 52 provided for receiving a SIMM 20, a second socket 54 provided for receiving a DIMM 40, a SIMM 20, a DIMM 40, signal transmission lines TL1 and TL2 for transmitting data between the memory controller 10 and the first socket 52, a resistor Rs connected between the memory controller 10 and the first socket 52 for matching impedance and a signal transmission line TL3 for transmitting data between the first socket 52 and the second socket 54.

The SIMM 20 contains a memory device 22, signal transmission lines TL4, TL5 for transmitting data between the memory device 22 and the first socket 52 and a stub resistor Rstub connected between the memory device 22 and the first socket 52 for matching impedance.

The DIMM 40 contains memory devices 42, 44, signal transmission lines TL6, TL7 for transmitting data between the memory devices 42, 44 and the second socket 54 and a stub resistor Rstub connected between the memory devices 42, 44 and the second socket 54 for matching impedance.

As shown in FIG. 1, the number of the memory devices acting as the loads is different in the SIMM and the DIMM. Accordingly, signal delay time is different in the SIMM and the DIMM.

In accordance with one embodiment of the present invention, the SIMM 20 has the shorter signal delay time in comparison with the DIMM 40 because the number of the memory devices in the SIMM is smaller than that in DIMM . Thus, the short signal delay time of the SIMM type memory module 20 is compensated by lengthening the length of the signal transmission lines TL4, TL5 in the SIMM 20. By configuring the

memory system in a way that the SIMM and the DIMM have the signal transmission lines with different lengths, respectively, the signal delay time difference caused by the different numbers of memory devices may be compensated and the signal integrity may be improved. Further, in the same manner, difference of signal delay time caused in the signal transmission line between the first socket where the SIMM is received and the second socket where the DIMM is received may be compensated too. Thus, the signal integrity is improved.

FIG. 2 and FIG. 3 illustrate waveforms for showing the signal integrity as the simulation results. FIG. 2 illustrates the waveforms showing the signal integrity of the memory system in which the SIMM and the DIMM has the same length of the signal transmission lines and FIG.3 illustrates the waveforms showing the signal integrity of the memory system in which the SIMM has the signal transmission line longer than that of the DIMM.

The signal integrity is measured from a pad formed on the memory device when the memory system is operated at 533 Mbps write speed. In the simulation, input capacitance of the memory devices 22, 42, 44 are set to 4 pF, a power supply voltage Vddq to 1.8V and distance between the first socket 52 and the second socket 54 to 0.45 inches.

FIG. 2(a) illustrates the signal integrity of the SIMM 20 and FIG. 2(b) illustrates the signal integrity of the DIMM 40. A signal transmission line TL6 of the memory system has a length of 0.8 inches that is the same as the length of the signal transmission line TL4. The stub resistances Rstub of the SIMM 20 and the DIMM 40 are the same. As

shown in FIG. 2, a great degree of skew is found. That is, the signal integrity is not good. At a voltage of 0.9V, the degree of the skew is 44ps in the SIMM 20 and 72ps in the DIMM 40, respectively. As described above, the signal integrity is greatly deteriorated due to the difference of the number of the loads such as the memory devices.

FIG. 3(a) illustrates the waveforms of the system integrity of the SIMM 20 and FIG. 3(b) illustrates the waveforms of the system integrity of the DIMM 40. In the simulation of FIG. 3, the lengths of the signal transmission lines TL6 and TL4 are 0.8 inches and 1.8 inches, respectively. Further, the length of the signal transmission line TL5 is the same as the length of the signal transmission line TL7. The stub resistances of the SIMM 20 and the DIMM 40 are the same.

As shown in FIGs. 3(a) and 3(b), since the signal transmission line TL4 formed in the SIMM 20 is longer than the signal transmission line TL6 formed in the DIMM 40, the degree of skew is greatly reduced. That is, the signal integrity is improved in comparison with the example of the FIG. 2(a) and FIG. 2(b). At the voltage of 0.9V, the degrees of skews are 18ps in the SIMM 20 and 50ps in the DIMM 40, respectively. In comparison with the simulation results of FIG. 2(a) and FIG. 2(b), the simulation results of FIG. 3(a) and FIG. 3(b) show reduction of skew to the extent of 26ps and 22ps in the SIMM 20 and the DIMM 40, respectively.

On the other hand, in the memory system containing the SIMM and the DIMM, the signal delay time difference caused by the signal transmission line distance between the first socket and the second socket may be compensated and the signal integrity is improved by forming the signal transmission line of the SIMM 20 to be longer than that

of the DIMM.

In the embodiment of the present invention describe above, the memory system includes a DIMM and a SIMM. However, the present invention may be applied to the memory system having more than one DIMM and more than one SIMM.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

[Effect of the invention]

In the embodiment of the present invention describe above, the memory system differentiate the length of transmission line in the SIMM type memory module from that of DIMM type memory module, thereby improves signal integrity. Furthermore the memory system can decrease a high frequency and is able to operate safely at higher speeds.

What is claimed is

1. A memory system having a SIMM and a DIMM, each containing a plurality of memory devices, wherein a signal transmission line in the SIMM type memory module is longer than a signal transmission line in the DIMM to compensate signal delay time difference caused by the different numbers of the memory devices contained in the SIMM and the DIMM, whereby improving signal integrity.

2. The memory system according to claim 1, wherein the memory system is able to compensate the signal delay time caused by signal transmission lines formed between a first socket for receiving the SIMM and a second socket for receiving the DIMM, whereby improving signal integrity.

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FIG. 1

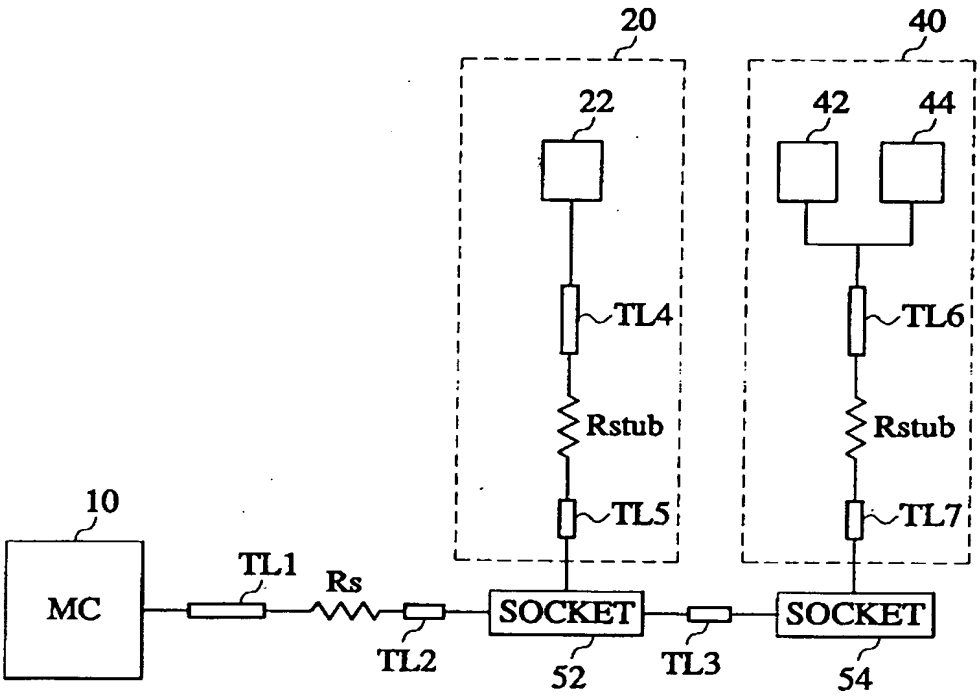

FIG. 2A

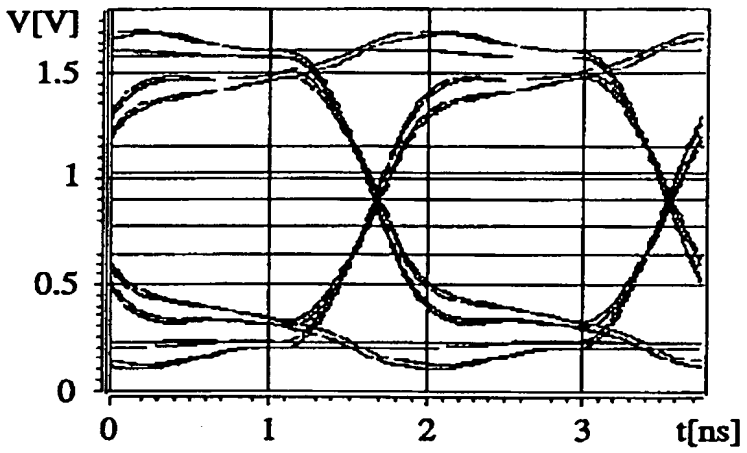

FIG. 2B

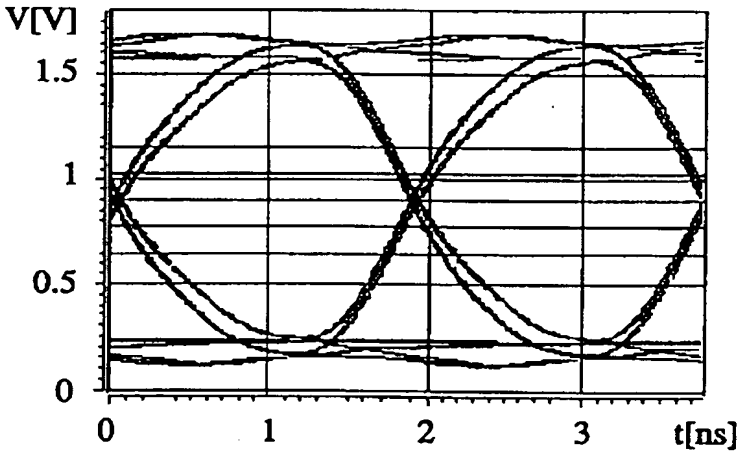

FIG. 3A

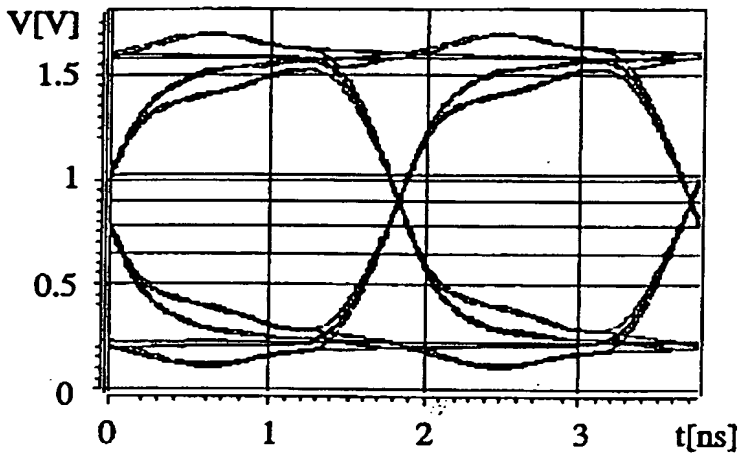

FIG. 3B